

The opinion in support of the decision being entered today was not written for publication in a law journal and is not binding precedent of the Board.

Paper No. 18

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte RICHARD M. BORN
and JACKSON L. ELLIS

Appeal No. 2001-2097
Application No. 09/052,849

ON BRIEF

Before RUGGIERO, GROSS, and SAADAT, Administrative Patent Judges.
RUGGIERO, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal from the final rejection of claims 1-20, which are all of the claims pending in the present application.

The claimed invention relates to a clock divider circuit for synthesizing a desired output clock waveform from multi-phase

input clock waveforms using combinations of integer and non-integer divisions of the input clocks. Included in the clock divider circuit are a first portion for performing integral division of the input clock waveforms in combination with a second portion for phase slip control which performs non-integer division of the source input waveforms.

Claim 1 is illustrative of the invention and reads as follows:

1. A clock divider circuit comprising:

an integral divider portion for dividing a source input clock signal by an integral divisor to produce a divided clock signal; and

a phase slip portion for applying a predetermined phase slip to said divided clock signal to produce a phase slipped divided clock signal as a non-integral division of said source input clock signal.

As the sole rejection by the Examiner before us, claims 1-20 stand finally rejected under 35 U.S.C. § 112, first paragraph, as being based on an inadequate disclosure.

Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the Brief (Paper No. 14) and Answer (Paper No. 15) for their respective details.

OPINION

We have carefully considered the subject matter on appeal, the rejection advanced by the Examiner, and the evidence and arguments relied upon by the Examiner as support for the rejection. We have, likewise, reviewed and taken into consideration, in reaching our decision, Appellants' arguments set forth in the Brief along with the Examiner's rationale in support of the rejection and arguments in rebuttal set forth in the Examiner's Answer.

It is our view, after consideration of the record before us, that Appellants' specification in this application describes the claimed invention in a manner which complies with the requirements of 35 U.S.C. § 112. Accordingly, we reverse.

As to the Examiner's assertion of lack of enablement of Appellants' disclosure, we note that, in order to comply with the enablement provision of 35 U.S.C. § 112, first paragraph, the disclosure must adequately describe the claimed invention so that the artisan could practice it without undue experimentation. In re Scarbrough, 500 F.2d 560, 566, 182 USPQ 298, 303 (CCPA 1974); In re Brandstadter, 484 F.2d 1395, 1404, 179 USPQ 286, 293 (CCPA 1973); and In re Gay, 309 F.2d 769, 774, 135 USPQ 311, 316 (CCPA 1962). If the Examiner has a reasonable basis for

questioning the sufficiency of the disclosure, the burden shifts to Appellants to come forward with evidence to rebut this challenge. In re Doyle, 482 F.2d 1385, 1392, 179 USPQ 227, 232 (CCPA 1973), cert. denied, 416 U.S. 935 (1974); In re Brown, 477 F.2d 946, 950, 177 USPQ 691, 694 (CCPA 1973); and In re Ghiron, 442 F.2d 985, 992, 169 USPQ 723, 728 (CCPA 1971). However, the burden is initially upon the Examiner to establish a reasonable basis for questioning the adequacy of the disclosure. In re Strahilevitz, 668 F.2d 1229, 1232, 212 USPQ 561, 563 (CCPA 1982); In re Angstadt, 537 F.2d 498, 504, 190 USPQ 214, 219 (CCPA 1976); and In re Armbruster, 512 F.2d 676, 677, 185 USPQ 152, 153 (CCPA 1975).

The Examiner has questioned the sufficiency of Appellants' disclosure in describing the structure of the components which comprise the clock divider circuit of the claimed invention. According to the Examiner (Answer, page 3), "... the invention is a complex structure and its operation is not apparent from the disclosure."

After careful review of the arguments of record, however, we are in agreement with Appellants' position as stated in the Brief. As asserted by Appellants (Brief, page 7), the Examiner, aside from a general allegation of insufficiency, has never

specifically indicated how Appellants' disclosure would not be enabling with regard to the particular clock divider circuitry recited in the appealed claims. For example, the Examiner has never indicated what is deficient in Appellants' disclosure related to the integral divider portions and phase slip portions of the claimed circuit structure. Our review of Appellants' disclosure, beginning at page 3, reveals a detailed description of the operation of the claimed clock divider circuit as well as a detailed gate level (Figures 3-6) description of the structure of the previously mentioned integral divider and phase slip portions. We are further persuaded by Appellants' argument (Brief, page 9) that clear evidence of the enabling nature of their disclosure is the inclusion in the original disclosure of a complete listing of the actual implementation of the claimed invention in the Verilog HDL language, which, as evidence on the record would indicate, is a hardware description language widely used by circuit design engineers.

In view of the above, we find that the Examiner has not established a reasonable basis for challenging the sufficiency of the instant disclosure. Accordingly, we will not sustain the

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rejection of claims 1-20 under the first paragraph of 35 U.S.C.
§ 112, and the Examiner's decision rejecting claims 1-20 is
reversed.

REVERSED

JOSEPH F. RUGGIERO)	
Administrative Patent Judge))	
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ANITA PELLMAN GROSS)	BOARD OF PATENT
Administrative Patent Judge))	APPEALS AND
)	INTERFERENCES
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MAHSHID D. SAADAT)	
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